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(54) Compressor surge detection system.

(57) In a compressor system, surge detection is provided by sensing the current of the motor driving the compressor and reading oscillations of the current about the average thereof and above and below two opposite threshold levels from such average current and counting the polarity changes within a time interval containing so many samples of the current and defining a sliding window.

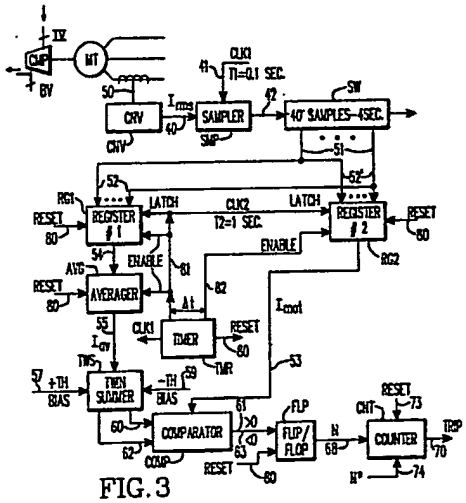

FIG.3

COMPRESSOR SURGE DETECTION SYSTEM

The invention resides in a surge detection system for a motor driven compressor characterized by sampling the motor current within a predetermined time interval and counting the occurrence of a predetermined minimum number of changes of polarity of the derived samples within such time interval.

The changes of polarity represent sharp deviations of the motor current in opposite directions from normal operation current magnitude, these deviations being due to motor loading behavior with the compressor and which manifest themselves as a result of a cyclical change of operation by the motor between motoring and regenerating modes, upon the occurrence of a surge. The deviations are measured by reference to the average current as sensed under normal operation and they are converted into an error condition when beyond a predetermined minimum deviation used as a threshold. The average current used as a reference is obtained by sampling the actual current and averaging the samples through a sliding window. Each error condition indicative of the threshold being exceeded is stored with an indication of its polarity. Changes of polarity are counted through a predetermined time interval as an indication of a surge condition. Protective measures are immediately triggered within the compressor system upon the detection of a surge condition.

The invention relates in general to compressor control, and more particularly to the prevention of the consequences of "surging" in such compressor control. "Surging" is a phenomenon caused by the compressor operating below a given amount of horse power or gas volume and the resulting occurrence of nonsteady state condition compounded by erratic control and an uncontrolled output.

The problem of surging and the prevention thereof have been explained in "Centrifugal and Axial Compressor Control by Gregory K. Mcmillan (The Instrument Society of America, 67 Alexander Drive, P.O. Box 12277, Research Triangle Park, NC 27709), 1983.

The present invention aims at an early detection of the occurrence of a surge, thereby providing an immediate opportunity of preventing the consequences thereof. Therefore, the invention distinguishes itself from the prior art methods by preventing the consequences of a surge by the timely and accurate detection of an occurring surge.

The invention is based on the magnitude of the current of the motor driving the compressor at the critical moment. The prior art has recognized the relationship existing between the volume of the compressed gas, or the pressure of the compressor, to the energy of the motor in operation, or its current. However, the object, there, has been to control the compressor as a function of the sensed current in order to prevent a surge, not to detect the surge, or in order to control the compressor in relation to the gas volume while observing the surge limit. See, for instance, U.S. Patents Nos. 3,778,695; 4,519,748 and 3,380,650, and also: "Surge Control For Multistage Centrifugal Compressors" by David F. Baker in Chemical Engineering May 31, 1982, pp. 117-122; "Improved Surge Control for Centrifugal Compressors" by N. Staroselsky and L. Ladin in Chemical Engineering May 21, 1979, pp. 175-184; and "Surge Control for Centrifugal Compressors" in Chemical Engineering December 25, 1972, pp. 54-62.

The invention will now be described, by way of example, with reference to the following drawings in which:

Figure 1 is a block diagram of the compressor control system according to the present invention;

Figure 2 is a graphic representation of the occurrence of a surge translated into polarity changes about two reference levels encompassing the average motor current, and as detected according to the present invention;

Figure 3 is a block diagram of the surge detection system according to the invention which is part of the compressor control system of Figure 1;

Figure 4 illustrates with curves the occurrence of the control signals during the operation of the system of Figure 3;

Figure 5 is a block diagram of the internal organization of the twin summer used in Figure 4 for the derivation of the thresholds to the comparator also of Figure 4;

Figure 6 is a block diagram illustrating the internal organization of the comparator and the trip signal derivation as taken from Figure 3;

Figures 7A to 7E are operational amplifier implementations illustrating the hardware interconnection between the elements of Figures 5 and 6;

Figure 8 is a flow chart explaining the steps involved in the operation of a microprocessor implementation of the circuit of Figure 3;

Figure 9 shows the solid state implementation of the circuit for the derivation of a signal representing the motor current;

Figures 10A to 10E are illustrating the solid state implementation of the circuit of Figure 3 when built around a microcomputer.

Referring to Figure 1, a compressor CMP is shown connected between the duct from the inlet and the duct to the outlet for a system using pressurized fluid. There is a separate duct having a normally closed bypass valve BV used in an emergency to blowoff the outlet pressure and override the load for protection. The inlet valve IV is placed at the inlet to control the incoming fluid, especially during startup. The compressor is driven by an electric motor, typically an AC motor supplied on three phases A,B,C from the AC power lines L1, L2, L3 through a contactor CNT. The system is controlled by a unit MCP including a computer, for instance a microcomputer, associated with digital circuitry including A/D and D/A converters interfaced with analog inputs and outputs, respectively. According to the present invention, motor current is sensed (from lines 50) and, after rectification and filtering (within block CNV), a signal representative of the rms of the current I of the motor is derived on line 40. This signal is inputted into the computer control unit MCP, from which is obtained an emergency trip signal on line 70 to a compressor control unit CCU in case alternate polarity changes in sufficient number have been detected, thereby denoting the occurrence of a surge. In response to such trip signal the compressor control unit will, by line 19, provide control for closing of the inlet valve IV, and by line 29 transmit a command to open the bypass valve BV. Control of the valves per se when required are well known in the compressor control field. They are controlled from the MCP unit, under normal control of the compressor unit CCU generally known, for instance for startup, pressure regulation, or merely to stop the overall operation.

Referring to Figure 2, the occurrence of a surge, is characterized by the motor current Imot erratically and cyclically oscillating between extreme values, up and down, as shown by curve (C). The gist of the present invention is to detect such oscillation and recognize a surge when oscillations occur a predetermined number of times. As explained hereinafter, high and low thresholds THi and THI are established above and below a normal operation representative signal selected to be the average current Iav occurring during a predetermined period, the latter chosen illustratively to be 4 seconds. When there is an oscillation, such threshold levels are exceeded (as shown between CD for the upper one, and EF for the lower one), alternatively one way and the other, and so many times. Indeed, should the value exceed one threshold more than once without encountering the opposite threshold, there would be no change of polarity, and therefore no count of an oscillation will take place. Imot (the sensed instantaneous value of the current), Iav (the average current for the period), THi (the higher threshold) and THI (the lower threshold) are determined within block MCP from the value of the current sensed and derived on line 40 of Figure 1. Illustratively, the thresholds THi and THI are at equal distance above and below line AVG of ordinate Iav, by an amount of +TH and-TH (represented in analog terms by voltages vhi and -vlo in Figures 7A to 7E as explained hereinafter). The current is sampled and N successive samples are held through a sliding window, the samples therein being on the basis of the well known "first in and last out" method. See for instance: U.S. patent Nos. 4,463,432 and 4,229,795. For the purpose of describing how a sliding window is implemented, these two patents are hereby incorporated by reference. Illustratively, it is assumed that 40 samples are collected within a period of 4 seconds, i.e. at a rate of 10 samples per second. When, within such predetermined time interval, so many alternative changes of polarity have been taking place (N* being the critical count in the illustration of Figures 3 and 4, hereinafter), the conclusion is that a surge is occurring and that measures have to be taken immediately in order to prevent undesirable consequences for the compressor. Commands for these measures are illustratively shown in Figure 1 to be control for closing of the inlet valve IV, by line 19, and for opening of the bypass valve BV, by line 29, as generally known.

Referring to Figure 3, a block diagram illustrates the internal organization in terms of functions, of the microprocessor unit MCP in its operation as a surge detector according to the present invention. The motor current is sensed from line 50 with respect to one phase of the motor (C), then rectified by an AC/DC converter CNV to provide on line 40 a signal 1 representative of the rms value of the motor current. From line 40, the motor current representative signal is applied to a sampler SMP controlled by a clock signal CLK1 derived on line 41 from a timer TMR, so as to so many times sample the motor current Imot, typically every 1/10 of a second. The sampling pulses are shown in Figure 4 under (a), ten sampling pulses appearing upon each passing of a second. These samples are passed by line 42 through a delay line SW, typically designed to contain 40 samples from the oldest to the latest received, thus, for a duration of 4 seconds. A clock signal CLK2 (shown under (c) in Figure 4), also derived from timer TMR, is applied by line 81 so as to command latching into two registers RGI and RG2 of data from the sampling window, via lines 52 for register #1 (RG1), via lines 52' for register #2 (RG2). Every second the registers are reset by line 80 from the timer. Therefore, every second within delay line SW, the 40 samples are being circulated so as to lose 10 samples at one end and to gain 10 samples at the other end, this will appear for the data latched into the registers.

Figure 4 shows under (b) three trains of 40 samples displaced by 1 second, or 10 samples, for successive instants (n-1), n, and (n + 1). Register #1 is enabled by line 81 so that data be passed by line 54 to an averager AVG. The average motor current is Iav, obtained on line 55 of Figure 3. After a time lag of Δt (typically of Δt = 200μs) following the instant that line 81 enables register #1 and the averager AVG, by line 82 timer TMR enables register #2, with the result that a sampled value of the motor current Imot is derived on line 53.

Iav is shown under (d) in Figure 4, the value being valid for a period of 1 second. The enabling signals of lines 81 and 82 are shown under (e) and (f), respectively. The time delay Δt, is required in order to allow the operation of the twin summer TWS in generating the reference values applied on lines 60 and 62 ahead of the derivation of Imot on line 53, the three lines being applied to comparator COMP. Twin summer TWS receives the two value of +TH and -TH of Figure 2, and this leads to the ordinates of thresholds THi and THI. The latter appear on lines 60 and 62, respectively. Comparator COMP relates Imot from line 53 to those two thresholds, and positive and negative polarity changes are generated on lines 66 and 67, one for the positive polarity being in relation to THi, the other for the negative polarity, thus, in relation to THI. A flip-flop FLP, reset by line 80, shifts from one state to the other when there is a change of polarity, and such occurrences are counted by a counter CNT responsive to line 68. A trip signal is generated on line 70 whenever the count N from line 68 reaches and exceeds a reference count N* applied on line 74. The counter is reset by line 73 upon each time interval of 1 second, thus, after each counting of Imot samples for a given Iav value under (d) in Figure 4. Figure 4 also shows under (g) how a count of N in such time interval may exceed the value N*. When this is the case, a logic 1 replaces the logic 0 on line 70 (under (h)) and a trip signal is applied to the compressor control unit CCU of Figure 1.

Figure 5 shows an analog implementation of the twin summer TWS first responsive to the Iav signal of lines 55 and 58 and to the +TH bias signal of line 57 with an output on line 62 of the signal $-Iav^{-}$, and secondly, responsive to the Iav signal of lines 55 and 56, and (after inversion between line 57 and line 59) to the -TH bias signal of line 59 with an output Iav^{+} on line 60. The signal of line 55 is assumed to be negative (-Iav) in order to match the circuitry of Figures 7A and 7B hereinafter. Figure 6 shows a hardware implementation of comparator COMP.

The circuits of Figures 5 and 6 are further illustrated in Figures 7A to 7E by an operational amplifier implementation. In Figure 7A, for one half twin summer, signal -Iav of line 56 combined with a voltage $-v_{hi}$ representing +TH applied on line 59. Therefore, on line 60 at the output of the operational amplifier OA is the resulting signal $(Iav + v_{hi}) = Iav^{+}$. Similarly, for the other half twin summer, on line 58 of Figure 7B is applied the signal -Iav, and on line 57 is applied the voltage $+v_{lo}$ representing -TH of Figure 2. Therefore, on line 62 at the output of the operational amplifier OA is the resulting signal $-(-Iav + v_{lo}) = -Iav^{-}$. Figure 7C shows the signal Imot of line 53 being inverted by device I so as to provide on line 53' the opposite value -Imot. Considering now Figures 7D and 7E which belong to comparator COMP of Figure 6, the outputted values of Figures 7A, 7B and 7C become here inputs, one leading in Figure 7D to $-(Iav^{+} - Imot) = A$ as output on line 61 for the corresponding operational amplifier OA, and the other leading in Figure 7E to $+(Iav^{-} - Imot) = B$ as output on line 63 for the corresponding operational amplifier OA. From the preceding, it appears that whenever on line 53' the sample -Imot is smaller than Iav^{+}, that is $Imot < (Iav + TH)$, like at point C on curve (C) of Figure 2, the output A, on line 61, is negative. Therefore, on line 66 into the flip-flop FF1 of Figure 6, the logic is low and the flip-flop is not triggered. This is because, for point C, Imot does not exceed the threshold THi. For point D, however, the quantity A is positive and line 61 becomes high, thereby triggering flip-flop FF1. In the same way, for point E on the curve of Figure 2, line 53 has Imot smaller than -Iav-, that is $Imot > (Iav - TH)$ and the output B, on line 63, is negative. This is because point E does not exceed the lower threshold. The logic of line 63 is low and flip-flop FF2 is not triggered. For point F, however, the logic of line 63 becomes high and flip-flop FF2 is triggered, because the threshold THI has been exceeded. Indeed, having triggered one flip-flop there will be a count of a change of polarity on line 68 of Figure 3 only if such triggering happens from one flip-flop to the other.

From Figures 2, 3, 5, 6 and 7A to 7E it appears that, according to the present invention, motor current is sampled every 0.1 second and a profile (or array) SW is maintained containing the latest 40 samples of motor current. The array is examined once each second to determine if a surge condition exists. A surge condition is determined by first calculating a "sliding" average value Iav of motor current based on the latest 40 samples of motor current stored in SW. The individual samples are then sequentially examined from the oldest to the newest with respect to the sliding average. A "polarity" change is maintained by defining a "positive" change in polarity as a motor current value in excess of the "sliding" average by a predetermined threshold amount and a "negative" change being a motor current value below the "sliding" average by a predetermined threshold. The number of times N that the "polarity" changes over this four second interval (40 samples) is then recorded and compared to a reference value N*. If the number N

exceeds or equals the value N*, then a surge condition exists.

Figure 6 shows comparator CMP associated with the flip-flops FF1 and FF2. The counter CONT here runs with the pulses of line 68 applied thereto, and the digital count (6 bits for instance) is compared with the reference count N* of lines 74 (also 6 bits). When the limit count N* has been reached, lines 72 at the output will have all Zero, so that a ONE will appear on line 70 at the output of the NOR device, indicating a surge.

Figure 8 is a flow chart explaining the software steps involved with the computer system MCP of Figure 1. The steps are as follows:

At 101 the question is raised whether the compressor is compressing air. If No, by line 104 the system goes to Return. If Yes, by 102 the next step is at 103 to ascertain what the average motor current (Iav) is for the present period. Then, by 105 the system goes to 106 where is determined what are the upper and lower thresholds (THi and THl, which are assumed to be +TH and -TH in Figure 2, and this is also what has been translated into voltages whi and vlo for the operational amplifier inputs of Figures 7A and 7B). Thereafter, by line 107, the system goes to 108 where the polarity counter (CNT in Figures 3 and 6) is set to zero for the start. Moreover at such initial step, the polarity is assumed to be the "positive" one. This means that the polarity last encountered by the flip-flops is assumed to be for a point on curve (C) of Figure 2 which was lastly above the upper threshold THi but is still above the lower threshold. This being done, by line 109 the system goes to block 110 where the question is: "whether for the oldest sample: Imot < (Iav-TH)?" This amounts to testing whether the polarity assumed to be "positive" is truly so. The question raised is whether the operative point is below the lower threshold rather than above. There are two possibilities. One is that the operative point for Imot remains above the lower threshold and there is no change of polarity, thus, the answer is NO on line 115. The other is that Imot has passed below the lower threshold, this means a change of polarity (from positive to negative). Therefore, by line 111 the system goes to block 112 where the polarity will be changed to the opposite one (the former assumption being wrongly to be positive). Such change of polarity is accounted for by counter CNT, at block 114, reached via line 113. As earlier stated, if at 110 the answer to Imot < (Iav - TH) is negated, by line 115 the system goes directly to line 116 without passing through a count at 114. Thereafter, by 120 the system goes to 121 where the next sample is taken into consideration. This will be done for all samples during the period (since there are 40 samples, it takes 4 second maximum to count at 114 the polarity changes and to see whether they reach and exceed the reference number N*), and it will be determined at 117 whether all samples have been tested. With each sample at 121, by line 122 the system goes to 123 where the test is whether Imot > (Iav + TH). This is, like for quantity A in Figure 7D, assuming that the operative point on curve (C) exceeds the upper threshold THi and, therefore, that the polarity is positive. If it is so, by line 126 the next step is to check whether the last polarity recorded was also positive. If it is so, the conclusion is that there is no polarity change and by line 131, the system bypasses block 112, going directly to block 121 by lines 116 and 120. Otherwise, by line 130 (which means a NO) a change of polarity is effected at 112 followed via line 113 by a count at 114. If there is a NO on 124, from block 123 the test becomes at block 125 whether Imot < (Iav - TH). This is like under Figure 7E with quantity B. If this is true, by line 127 there should be a negative polarity. If at 129 there is indeed already a negative polarity, no change of polarity (triggering) need to take place and the system by line 131 goes directly to lines 116, 120 onto block 121 for the next sample of Imot. If the actual polarity was positive, block 129 will say NO on line 130, thereby indicating a change of polarity (triggering). Such change is acknowledged and counted at 114. This goes until the last sample acknowledged at 117. Then, by line 118 the test becomes at 119 whether N* such changes have been taking place. If so, by line 132 (with a YES) and via line 134 (if at 133 a surge has not already been detected) the system goes to block 135 where the flag is set to indicate a "surge". Then, by lines 138 and 104 the system goes back to RETURN. The inlet valve and bypass valve control software logic at 141 is the one which by line 139 initiates at 101 the routine just considered. When a "set surge flag" logic has been received from line 138 and passed to RETURN by line 104, this is acknowledged by line 140 within block 141. The fact is established at 143 in another routine which by line 70 generates the command to the compressor control unit CCU of Figure 1. Otherwise, that is, if there has been no surge flag set in the course of the time interval defined at 117 and as ascertained at 133, normal control will take place from block 143 to block CCU. The questions and answers between the two routines, namely between lines 139 and 140 is about 3 ms. If there has been no surge detection, there is a NO from block 119 with a return by line 136, and if there has been a surge already detected, there will be a return from block 133 via line 137. If the reference count N* has not been reached at 119, while incrementing counter CNT at 114, the decision is to return via line 104. If this is the first time that polarity changes have equated or exceeded N*, the command is to reset the surge detection in 3 seconds, to set the surge flag, and to set the other bits. This is done at 135 and the system returns by 104 for further testing of a possible surge occurrence.

The flow chart steps are performed by the computer control unit MCP illustrated by Figures 9 and 10A to 10E. The computer control unit includes a microcomputer MICRO (in Figure 10A). Figure 9 shows the derivation of the motor current representative signal, on line 40, after conversion by converter CNV of the AC current of the motor. The motor current signal is passed thereafter on line 240 toward line 240' of Figure 10C at the input of the A/D converter section of the computer control unit. AD converter AD1 there generates on line 203 the ADIN data for treatment by the microcomputer. Two RAM devices are shown in Figure 10B, one volatile, the other non-volatile. Line 203 of Figure 10C goes to a latch LTC1 (Figure 10B) which passes data, via data bus 202 (ADBUS), to a RAM device (RAM1) that is addressed by address bus 201 (ADDRESS BUS) from the MICRO (Figure 10A). One of these two RAM devices is equivalent to registers RG1 and RG2 of Figure 3. Figure 10B also shows a latch LTC2 which is passing data from RAM1, as well as from another RAM device (RAM2), on line 204 (DAOUT) onto digital to analog converters DA1 and DA2 outputting analog signals on lines 219' and 229' (Figure 10D) when line 70 (Figure 1) commands tripping of the inlet valve and the bypass valve (IV and BV), respectively. The commands of lines 219' and 229' are passed on lines 219 and 229, respectively, which are similar to lines 19 and 29 of Figure 1. The internal operation of the microcomputer MICRO handling data in digital form as received or as generated is according to the flow chart of Figure 8. The solid state devices used for such software operation which have been labelled in the Figures are well understood as to their nature and mode of operation. Thus, the motor current analog value AIN carried on line 240 of Figure 9 is brought via lines 240 and 240' onto the A/D converter AD1 to become its digital counter part ADIN of line 203 of Figure 10C. From there ADIN is stored in latch LTC1 of Figure 10B. The microcomputer MICRO of Figure 10A receives or generates data in its various operations which are transmitted along ADBUS line 202 from or onto the ROM of Figure 10A, the registers (RG1 and RG2) implemented as RAM's (RAM1 in this case) and/or the latches LTC1, LTC2 of Figure 10B, the address bus (line 201) making the selection of the locations in the devices. A signal +vREF is shown on line 205 which is used for scaling of the value of the positioning signals for the inlet valve (IV) on line 219 (which matches line 19 of Figure 1) and for the bypass valve (BV) on line 229 (which matches line 29 of Figure 1).

IDENTIFICATION OF REFERENCE NUMERALS USED IN THE DRAWINGS

LEGEND	REF. NO.	FIGURE
COMPRESSING AIR	101	8
DETERMINE I_{av} FOR THIS PERIOD	103	8
DETERMINE TH_I AND TH_I	106	8
ZERO POLARITY COUNTER, & INITIALIZE POLARITY TO +	108	8
I_{mot} SAMPLE (OLDEST) < (I_{av} - TH)	110	8
COMPLEMENT POLARITY SIGN	112	8
INCREMENT POLARITY COUNTER	114	8
ARE ALL MOTOR CURRENT SAMPLES TESTED	117	8
NUMBER OF POLARITY CHANGES > N*	119	8
GET NEXT MOTOR CURRENT SAMPLE	121	8
MOTOR CURRENT SAMPLE > (I_{av} - TH)	123	8
MOTOR CURRENT SAMPLE < (I_{av} - TH)	125	8
POLARITY > 0	128	8
POLARITY < 0	129	8
SURGE ALREADY DETECTED	133	8
SIGNAL TO RESET SURGE DETECTION IN 3 SECONDS + SET SURGE FLAG + SET OTHER BITS	135	8
IV/BV CONTROL SOFTWARE LOGIC	141	8
SURGE FLAG SET	143	8

Claims

1. A surge detection system for a compressor driven by an electric motor characterized by: means for deriving a signal representative of the motor current magnitude; means responsive to said current representative signal for deriving a reference signal representative of the average magnitude thereof during a predetermined time interval; means responsive to said reference signal and to said current representative signal for detecting a deviation from said average magnitude by a predetermined amount in one direction; means responsive to said reference signal and to said current representative signal for detecting a deviation from said average magnitude by said predetermined amount in the opposite direction; means for counting successive said deviations in opposite directions during another predetermined time interval for deriving a representative count; and means responsive to a reference count and to said counting means for generating a signal characteristic of a surge condition when said representative count matches said reference count.

2. The surge detection system of claim 1 including means for protection against operation under surge and means responsive to said surge condition characteristic signal for triggering the protection means.

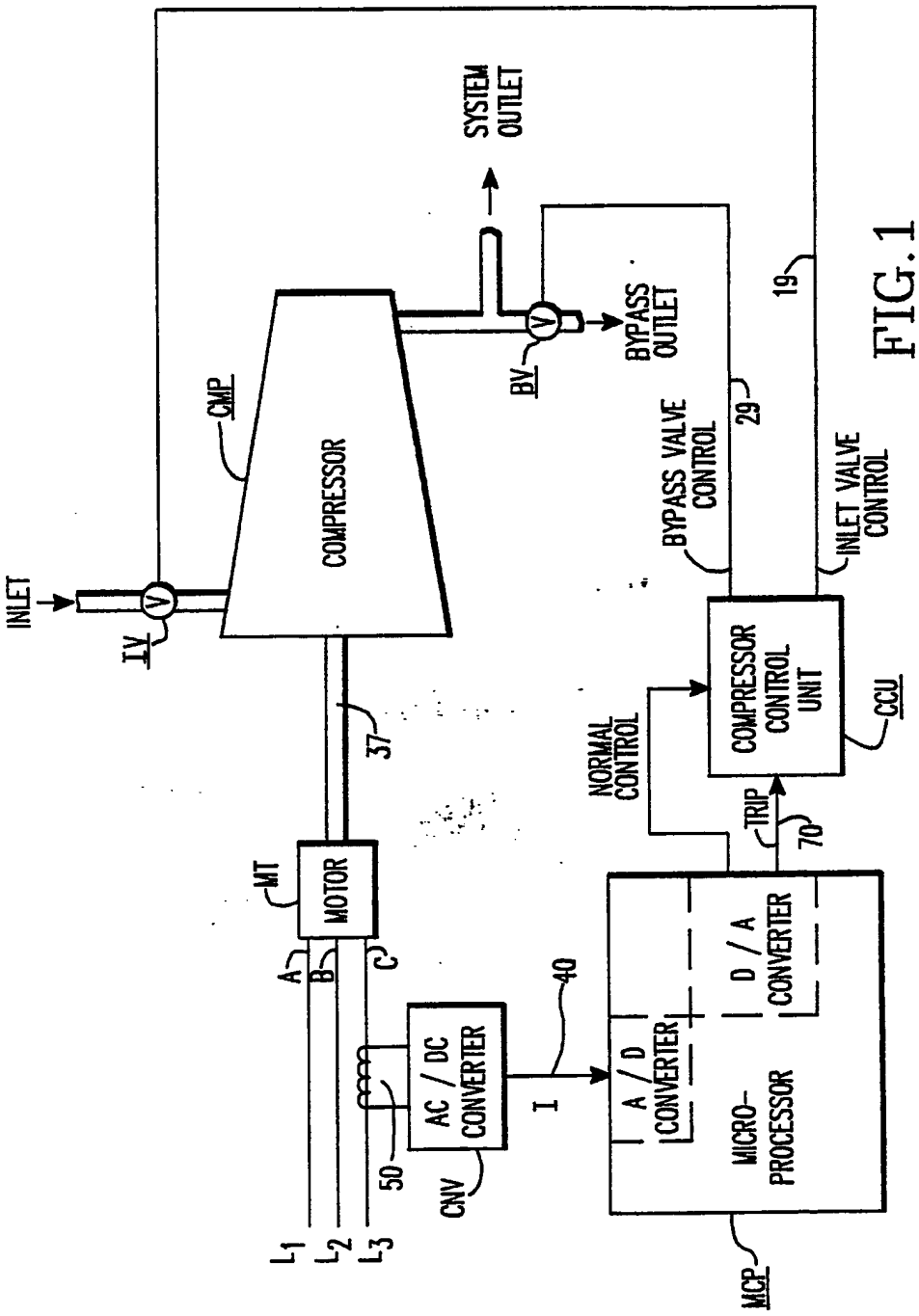
SYSTEM OUTLET
BYPASS OUTLET
BV
CMP
COMPRESSOR
INLET
IV
BYPASS VALVE CONTROL
29
19
INLET VALVE CONTROL
COMPRESSOR CONTROL UNIT
CCU
NORMAL CONTROL
TRIP
70
37
MT
MOTOR
A
B
C
AC / DC CONVERTER
CNV
50
40
I
A / D CONVERTER
D / A CONVERTER
MICRO-PROCESSOR
MCP
L1
L2
L3

FIG. 1

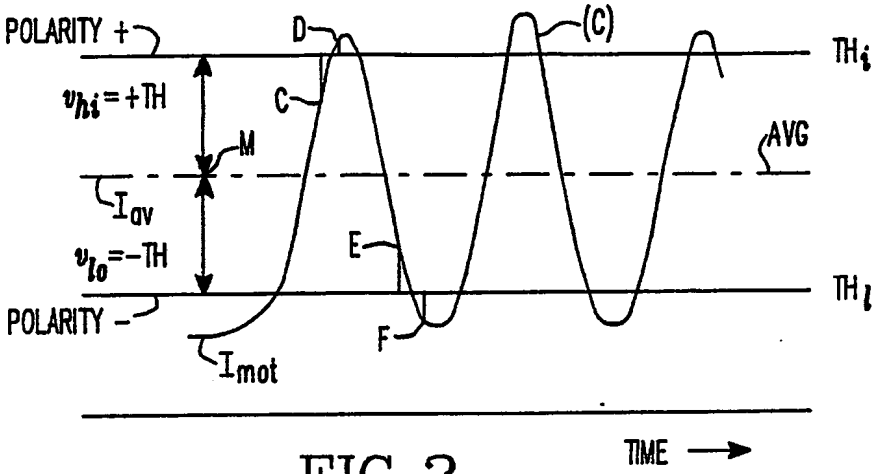
POLARITY +
D
(C)
TH$_i$
v_{hi} = +TH
C
M
AVG
I_{av}
v_{lo} = -TH
E
TH$_l$
POLARITY -
F
I_{mot}
TIME

FIG. 2

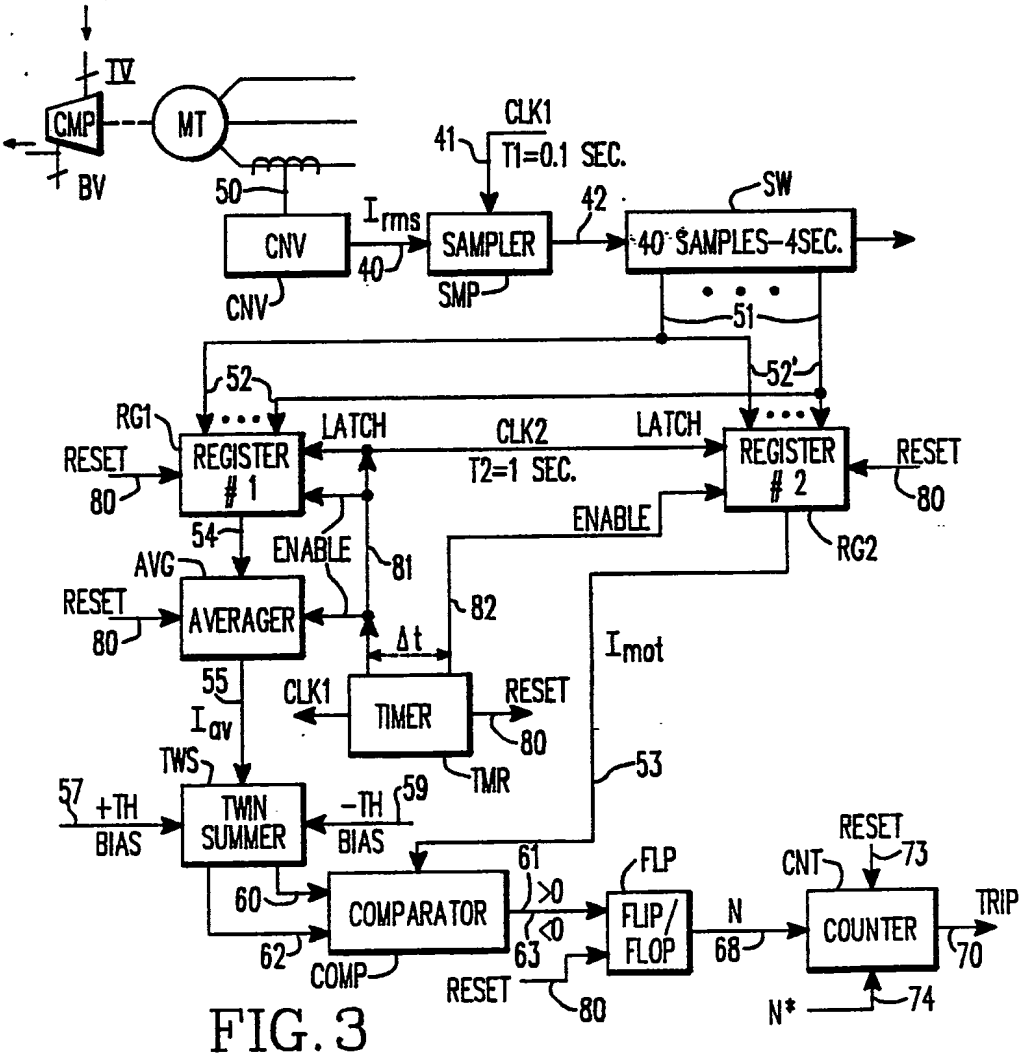
IV
CMP
MT
BV
50
CLK1
41
T1=0.1 SEC.
SW
42
CNV
I_{rms}
40
SAMPLER
40 SAMPLES-4SEC.
CNV
SMP
51
52
52'
RG1
LATCH
CLK2
LATCH
RESET
REGISTER # 1
T2=1 SEC.
REGISTER # 2
RESET
80
80
54
ENABLE
81
ENABLE
RG2
AVG
RESET
AVERAGER
82
80
Δt
I_{mot}
55
CLK1
TIMER
RESET
I_{av}
80
TWS
TMR
53
57
+TH
BIAS
TWIN SUMMER
-TH
59
BIAS
RESET
61
FLP
CNT
73
60
COMPARATOR
>0
<0
FLIP/ FLOP
N
68
COUNTER
TRIP
70
62
63
COMP
RESET
80
N*
74

FIG. 3

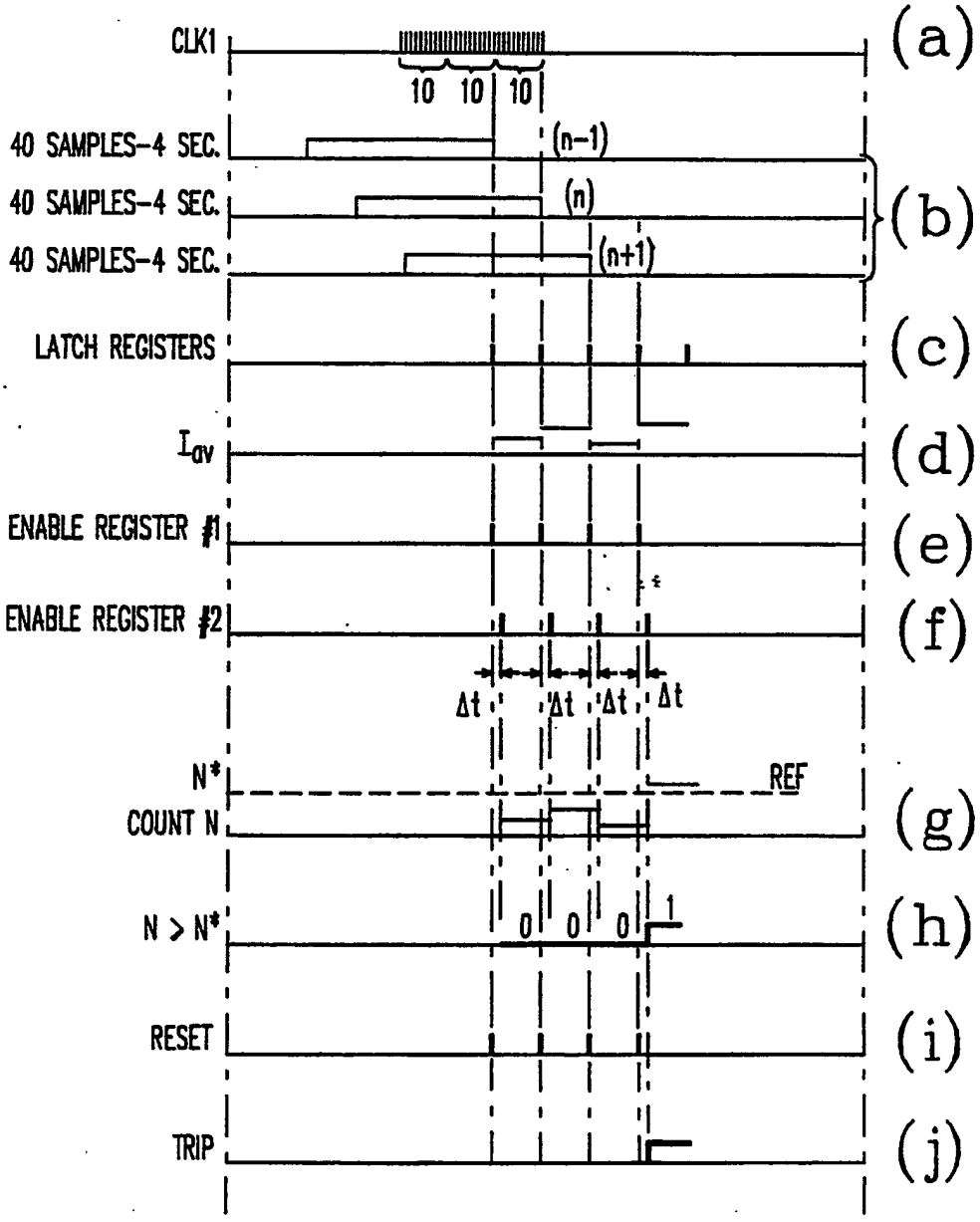
CLK1
10 10 10
(a)
40 SAMPLES–4 SEC.
(n–1)
40 SAMPLES–4 SEC.
(n)
40 SAMPLES–4 SEC.
(n+1)
(b)
LATCH REGISTERS
(c)
I_{av}
(d)
ENABLE REGISTER #1
(e)
ENABLE REGISTER #2
(f)
Δt Δt Δt Δt
N*
REF
COUNT N
(g)
N > N*
0 0 0 1
(h)
RESET
(i)
TRIP
(j)

FIG. 4

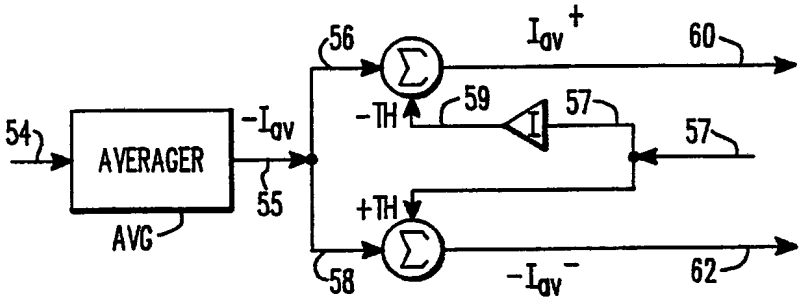
54
AVERAGER
AVG
55
$-I_{av}$
56
I_{av}^+
60
-TH
59
57
57
+TH
58
$-I_{av}^-$
62

FIG. 5

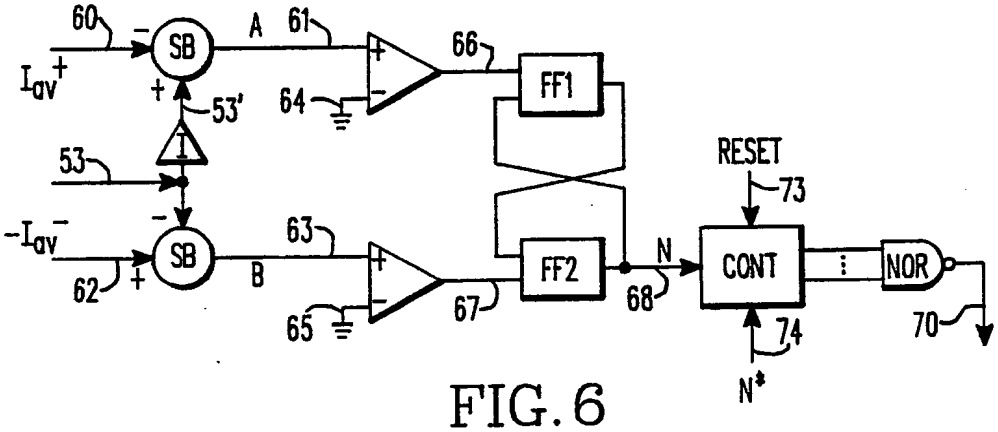
60
SB
A
61
I_{av}^+
53'
64
66
FF1
53
RESET
73
$-I_{av}^-$
62
SB
B
63
65
67
FF2
N
68
CONT
NOR
70
74
N^*

FIG. 6

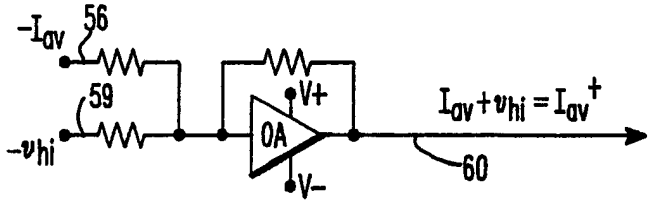

FIG. 7A

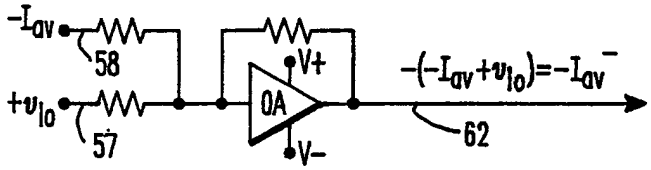

FIG. 7B

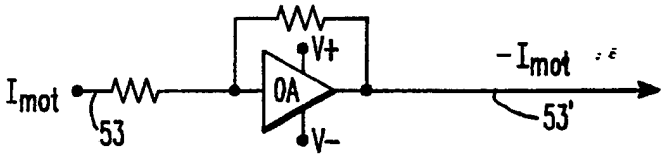

FIG. 7C

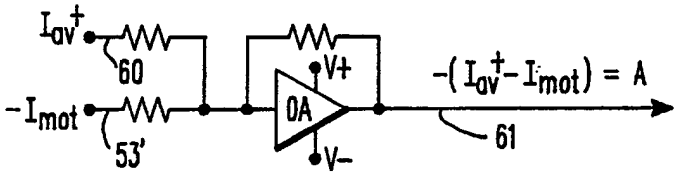

FIG. 7D

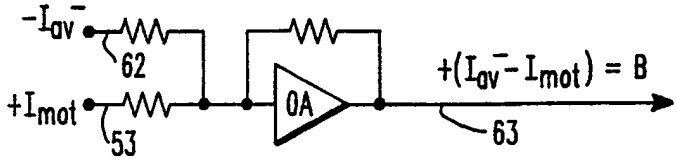

FIG. 7E

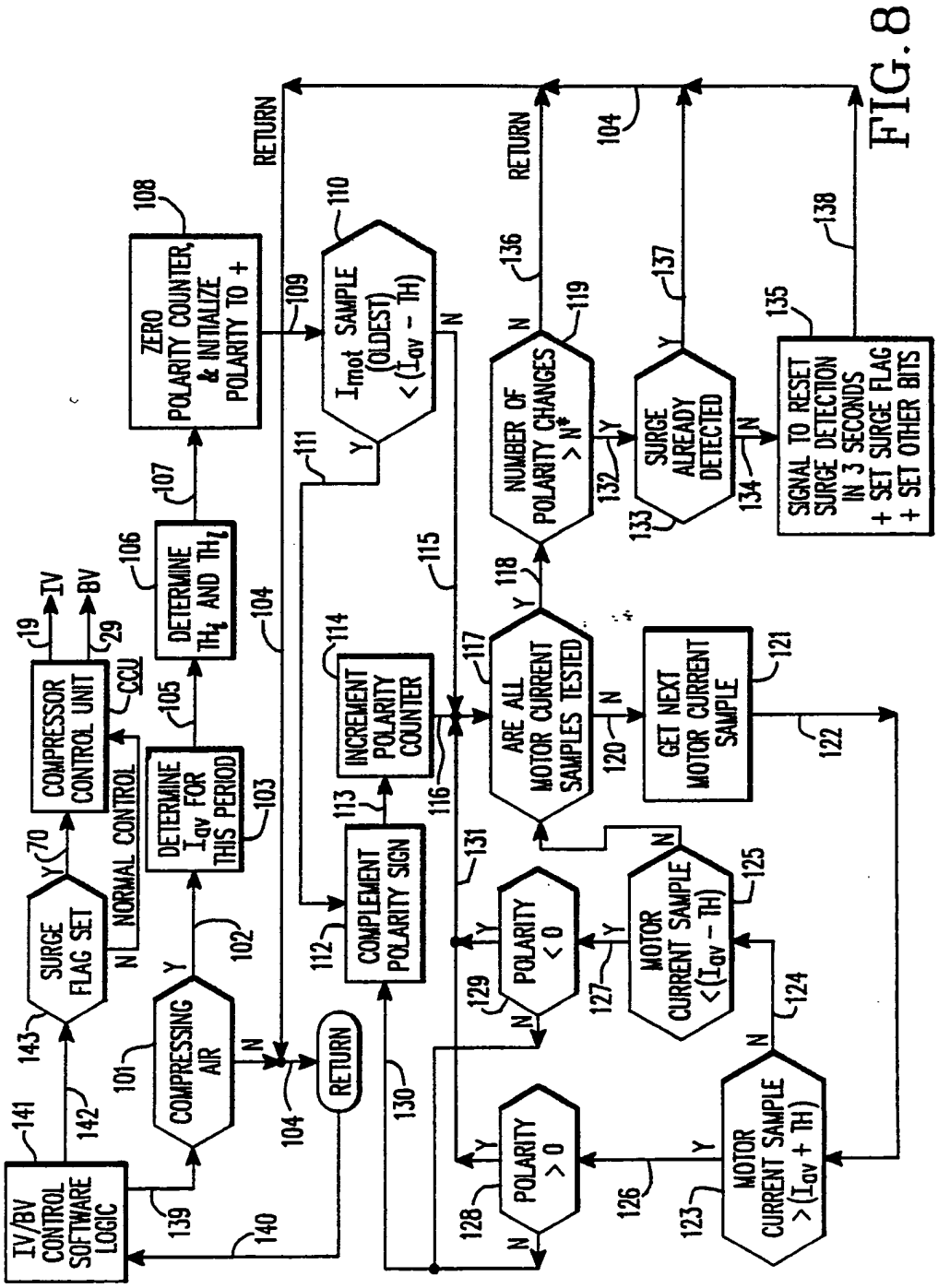
IV/BV CONTROL SOFTWARE LOGIC
141
142
143
SURGE FLAG SET
Y
70
N
NORMAL CONTROL
COMPRESSOR CONTROL UNIT
CCU
19
IV
29
BV
COMPRESSING AIR
101
Y
N
DETERMINE I_{av} FOR THIS PERIOD
102
103
DETERMINE TH_1 AND TH_2
105
106
ZERO POLARITY COUNTER, & INITIALIZE POLARITY TO +
107
108
RETURN
104
I_{mot} SAMPLE (OLDEST) $< (I_{av} - TH)$
109
110
111
Y
N
INCREMENT POLARITY COUNTER
114
115
116
COMPLEMENT POLARITY SIGN
112
113
130
131
ARE ALL MOTOR CURRENT SAMPLES TESTED
117
118
Y
N
GET NEXT MOTOR CURRENT SAMPLE
120
121
122
NUMBER OF POLARITY CHANGES $> N^*$
119
136
RETURN
SURGE ALREADY DETECTED
132
133
137
SIGNAL TO RESET SURGE DETECTION IN 3 SECONDS + SET SURGE FLAG + SET OTHER BITS
134
135
138
POLARITY < 0
129
127
MOTOR CURRENT SAMPLE $< (I_{av} - TH)$
125
124
POLARITY > 0
128
126
MOTOR CURRENT SAMPLE $> (I_{av} + TH)$
123

FIG. 8

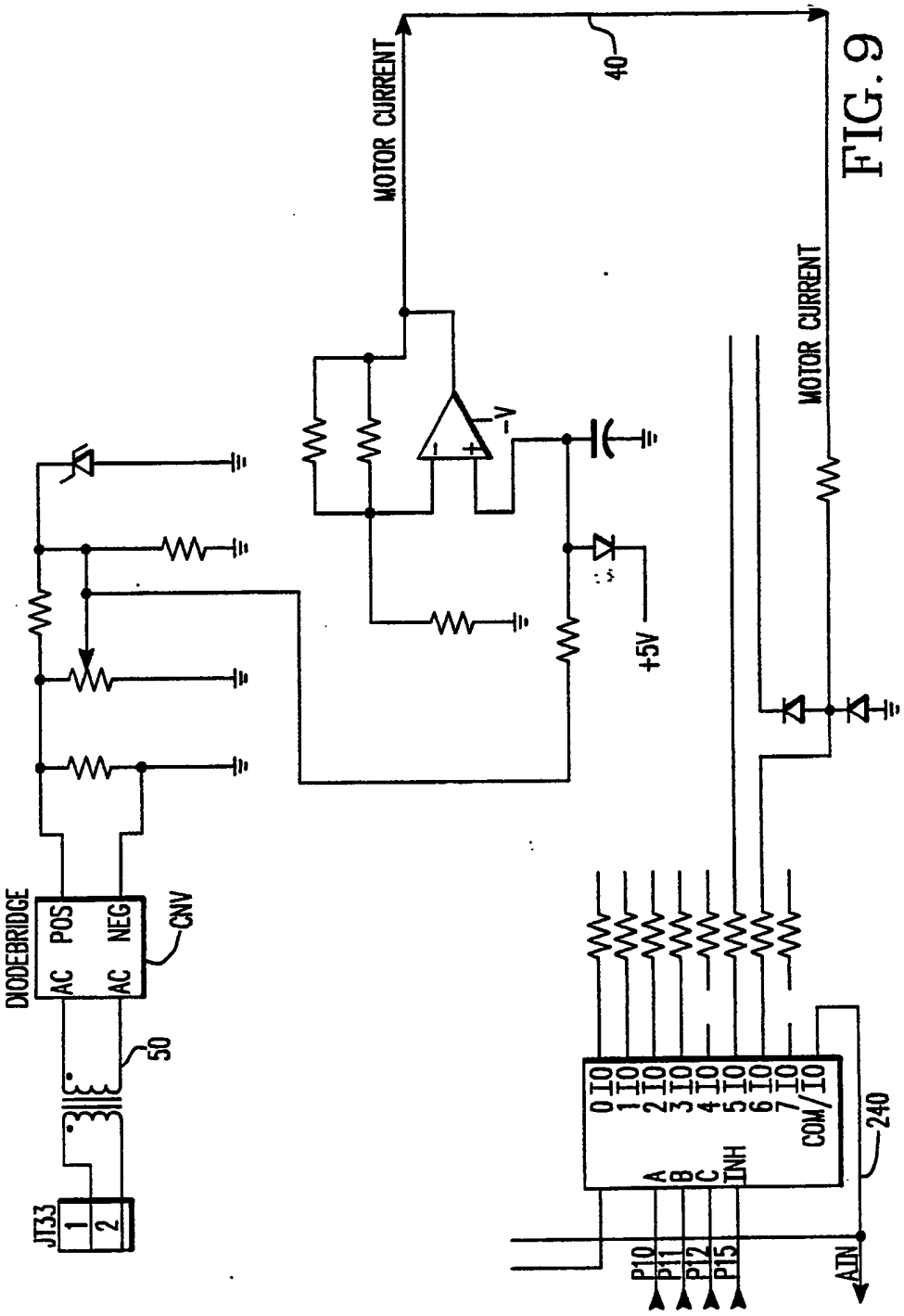
MOTOR CURRENT
40
MOTOR CURRENT
-V
+5V
DIODEBRIDGE
AC
POS
NEG
AC
CNV
50
JT33
1
2
0 IO
1 IO
2 IO
3 IO
4 IO
5 IO
6 IO
7 IO
COM/IO
240
A
B
C
INH
P10
P11
P12
P15
AIN

FIG. 9

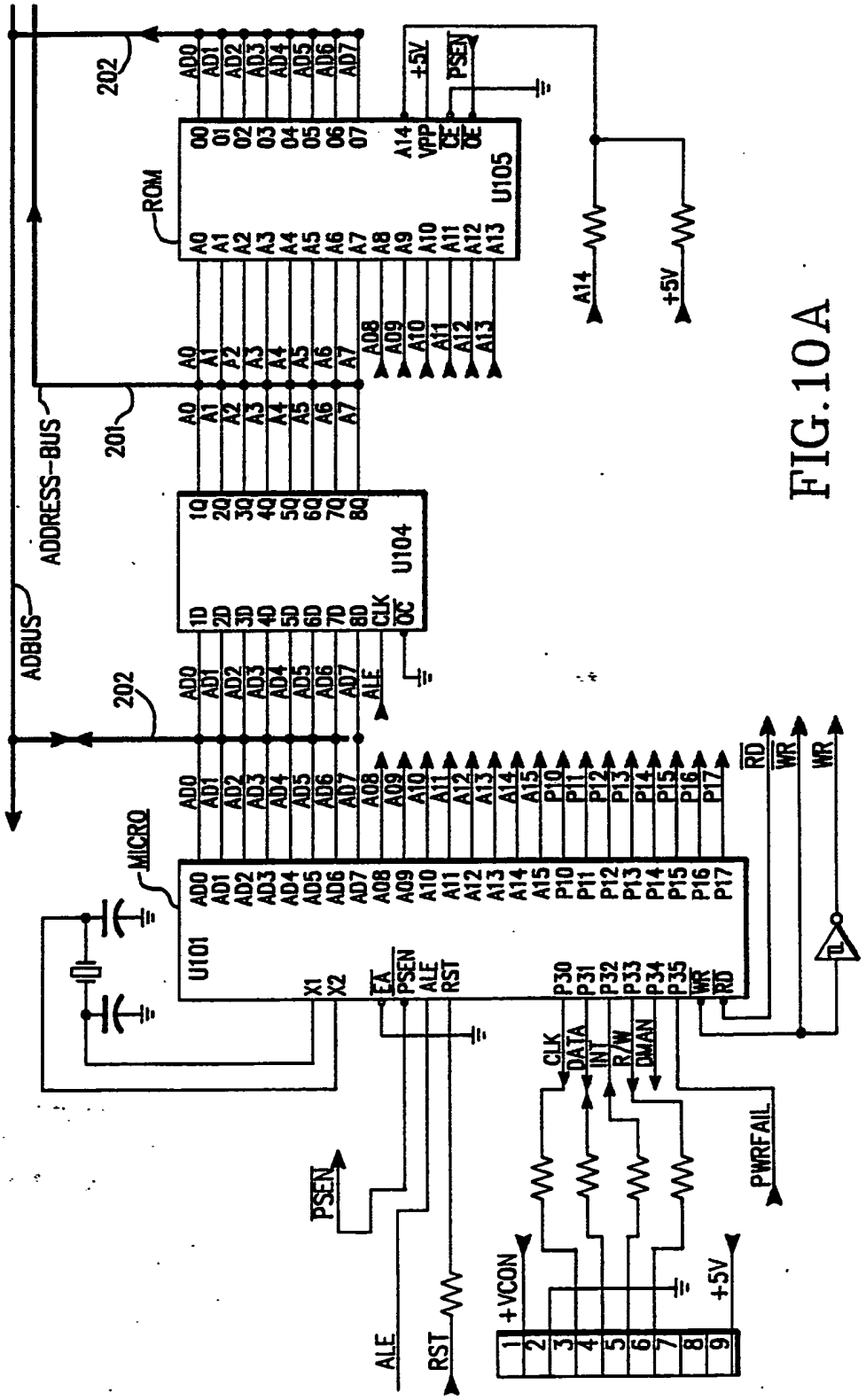
202
ADDRESS-BUS
201
ADBUS
202
MICRO
ROM
U105
U104
U101
+5V
PSEN
A14
VPP
ALE
RST
EA
X1
X2
RD
WR
CLK
DATA
INT
R/W
DMAN
PWRFAIL
+VCON
1
2
3
4
5
6
7
8
9

FIG.10A

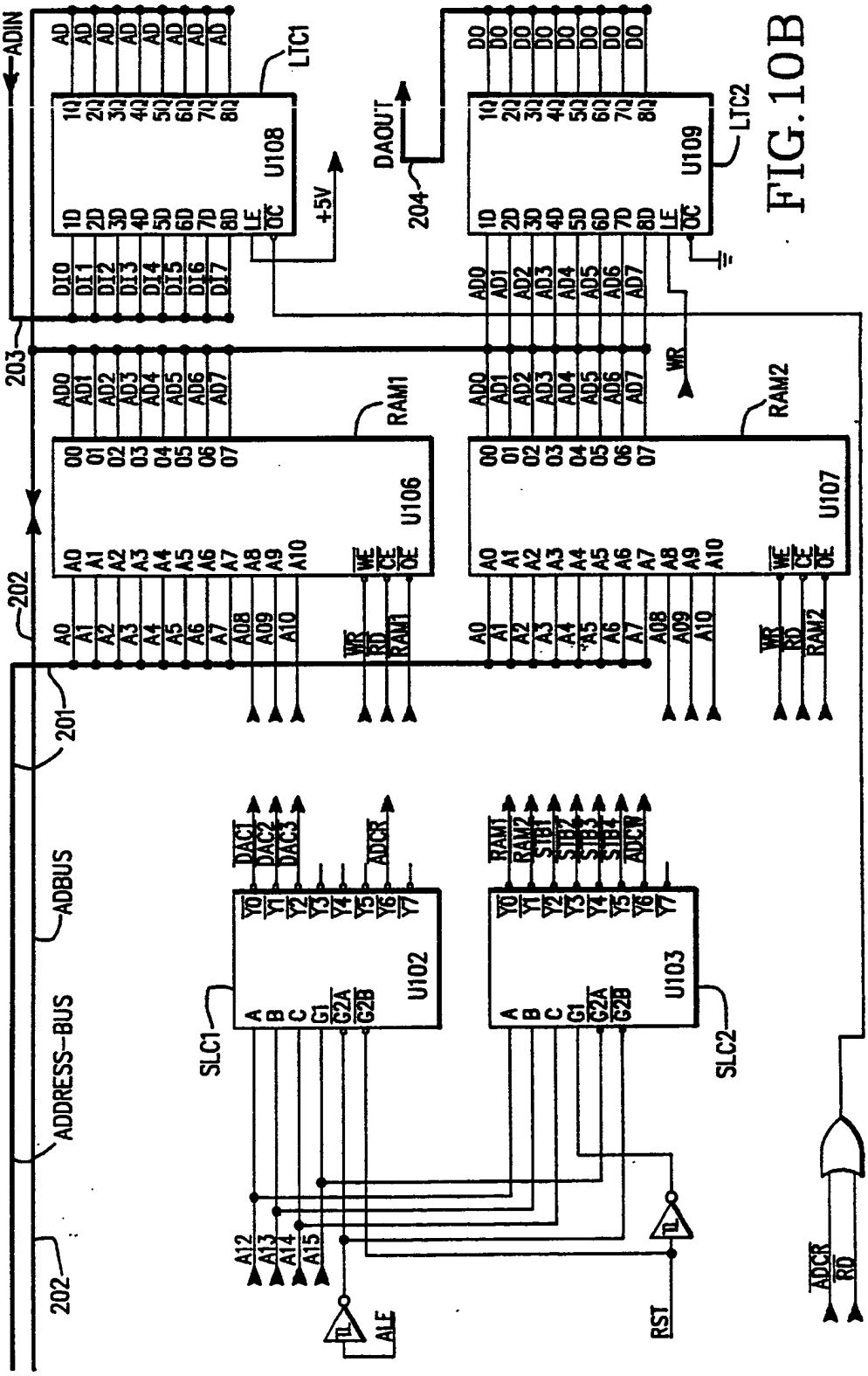
ADIN
LTC1
U108
DAOUT
204
LTC2
U109
+5V
203
WR
RAM1
U106
RAM2
U107
202
201
ADBUS
ADDRESS-BUS
202
U102
U103
SLC1
SLC2
A12
A13
A14
A15
ALE
RST
ADCR
RD

FIG.10B

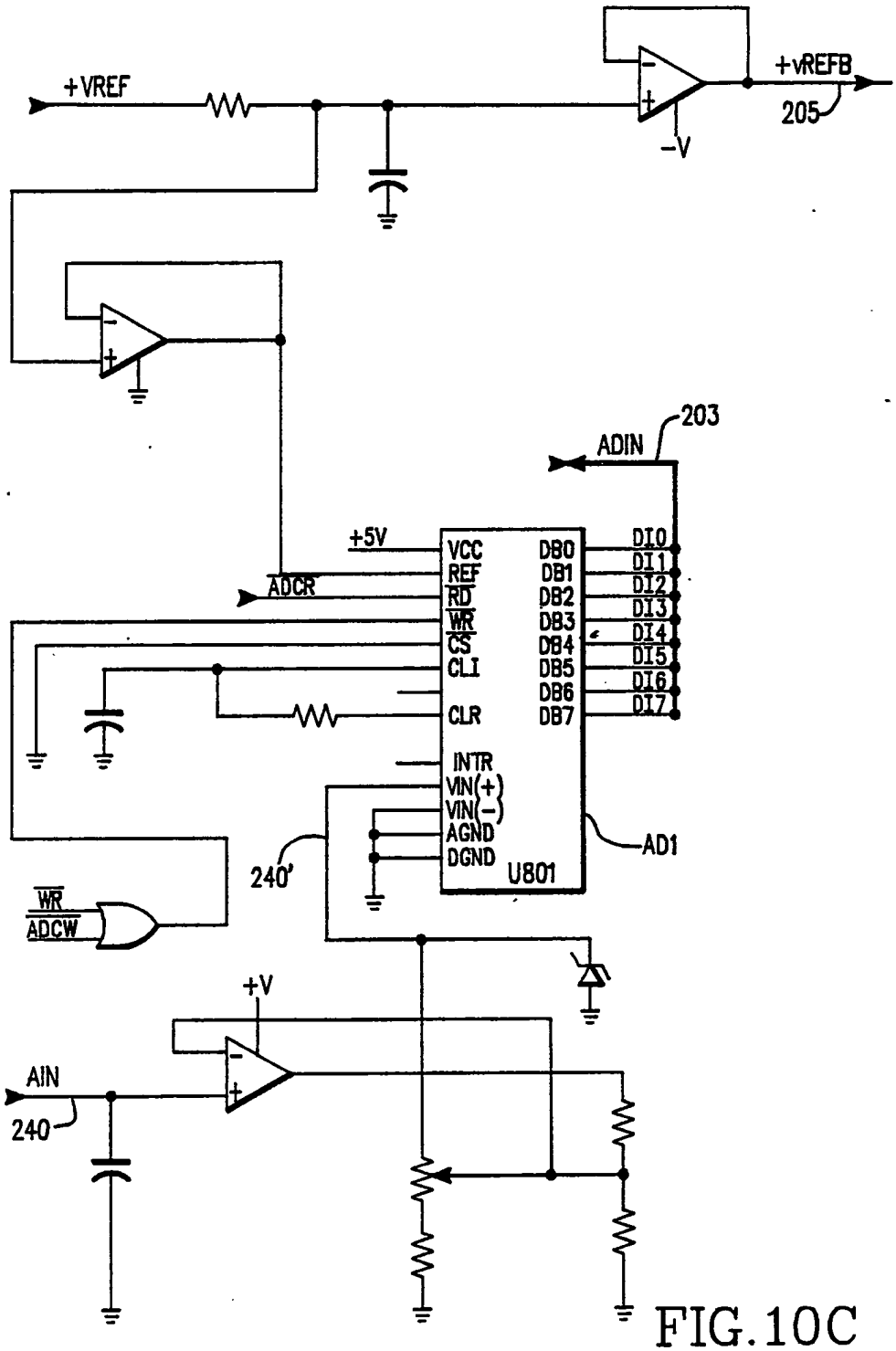
+VREF
+vREFB
205
-V
203
ADIN
+5V
VCC
REF
RD
WR
CS
CLI
CLR
INTR
VIN(+)
VIN(-)
AGND
DGND
U801
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
ADCR
AD1
240'
WR
ADCW
+V
AIN
240

FIG.10C

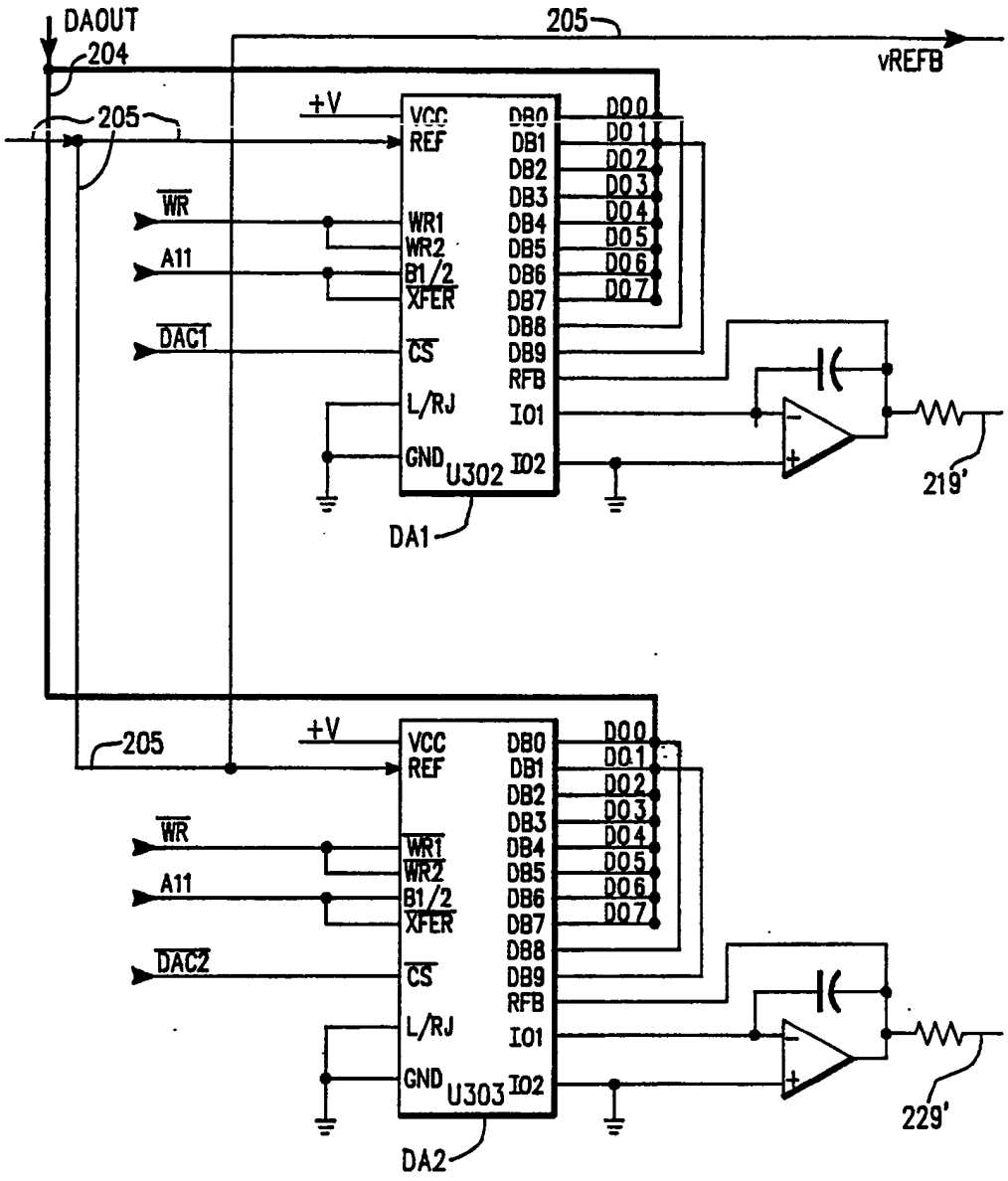
DAOUT
204
205
vREFB
205
+V
VCC
REF
WR
WR1
WR2
A11
B1/2
XFER
DAC1
CS
L/RJ
GND
U302
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
RFB
IO1
IO2
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
219'
DA1
205
+V
VCC
REF
WR
WR1
WR2
A11
B1/2
XFER
DAC2
CS
L/RJ
GND
U303
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
RFB
IO1
IO2
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
229'
DA2

FIG.10D

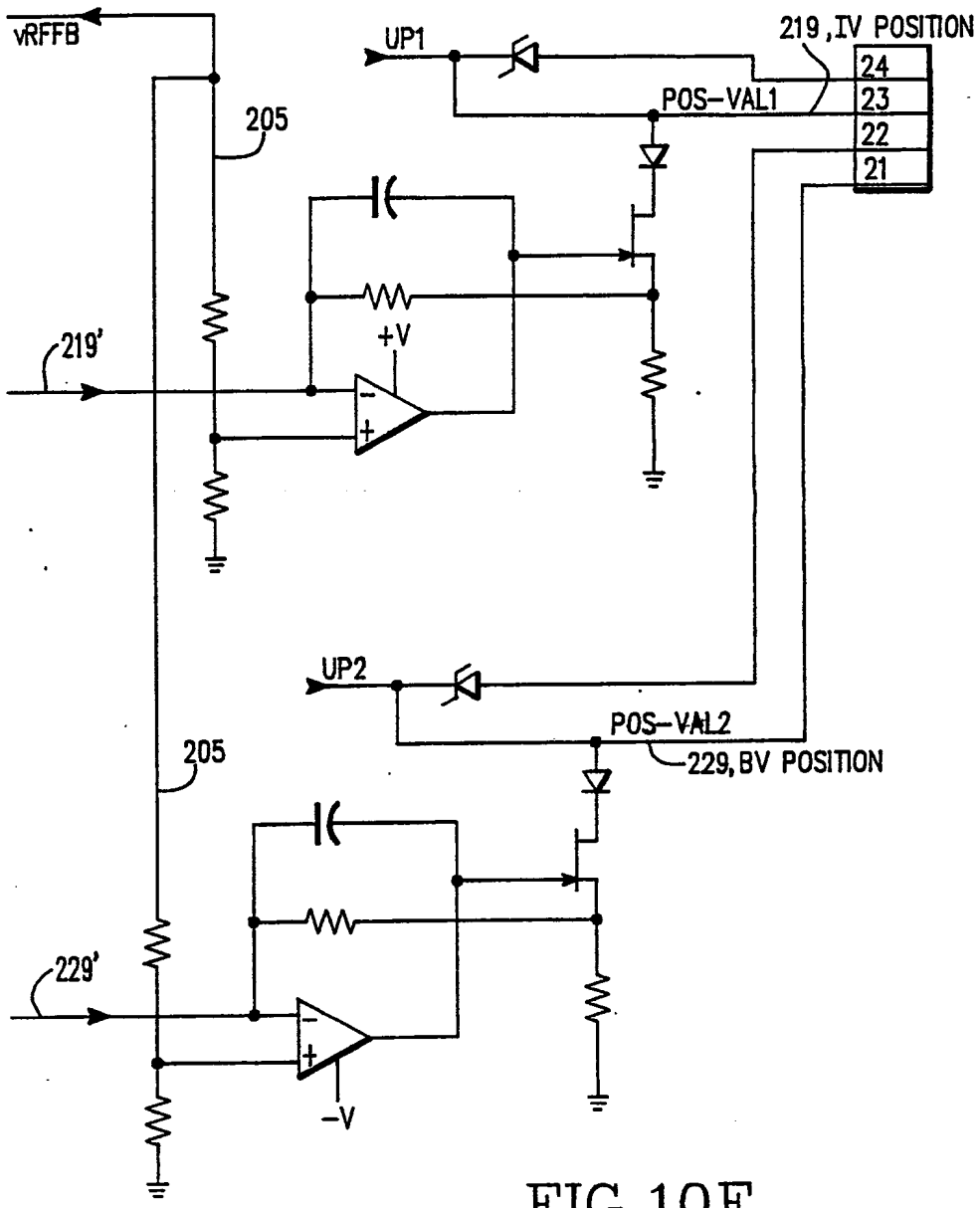
vRFFB
205
UP1
219, IV POSITION
24
23
22
21
POS-VAL1
219'
+V
UP2
POS-VAL2
229, BV POSITION
205
229'
-V

FIG.10E